In the Claims

Claims 1-17 have been cancelled with this response.

18. (Newly Added) An apparatus (302) for performing dynamically scalable single instruction multiple data (SIMD) operations comprising:

a first vector arithmetic logic unit (402) operably coupled to a first data vector (VRA) from a first input data bus, a second data vector (VRB) from a second vector data bus, and a third data vector (VRC) from a third vector data bus to produce a first vector result (VRD) wherein the first vector functional arithmetic logic unit (402) performs individual conditional operations on fields of VRA and VRB to produce VRD, and wherein the conditional operations are based on VRC;

a second vector arithmetic logic unit (401) operably coupled to the first data vector (VRA) from the first input data bus, the second data vector (VRB) from the second input data bus, and to the first vector arithmetic logic unit, wherein the individual conditional vector operations in the first vector arithmetic logic unit are conditionally controlled by a vector result from the second vector arithmetic logic unit.

19. (Newly Added) The apparatus of claim 18 wherein the first vector arithmetic logic unit performs addition and subtraction.

20. (Newly Added) The apparatus of claim 19 wherein the second vector arithmetic logic unit performs subtraction.

21. (Newly Added) The apparatus of claim 18, wherein a sign of the vector result from the second vector arithmetic logic unit controls individual conditional SIMD field operations of the first vector arithmetic unit within a single clock cycle.

22. (Newly Added) The apparatus of claim 18, wherein the vector result from the second vector arithmetic logic unit are fed back as a vector input to the first vector arithmetic logic unit within a single clock cycle.

23. (Newly Added) The apparatus of claim 18, wherein the vector result from the second vector arithmetic logic unit is output as a second vector result (VRE).

24. (Newly Added) An apparatus (302) for performing dynamically scalable SIMD operations, the apparatus (302) comprising:

a first vector arithmetic unit (402) having a first, second, and third data vector as inputs, the first vector arithmetic unit capable of performing at least vector addition and subtraction operations, wherein individual SIMD field operations in the first vector arithmetic unit are conditionally controlled by at least a portion of the third data vector input; and

a second vector arithmetic unit (401) operably coupled to the first vector arithmetic unit.

25. (Newly Added) The apparatus of claim 24 wherein the first vector arithmetic unit performs at least vector addition and subtraction.

26. (Newly Added) The apparatus of claim 24, wherein packed bitwise values of the third data vector alter individual SIMD field operations of the first vector arithmetic unit within a single clock cycle.

27. (Newly Added) The apparatus of claim 24, wherein a dynamically scalable vector addition and subtraction operation is performed by the first and the second vector arithmetic units and output simultaneously, within a same clock cycle.

28. (Newly Added) The apparatus of claim 24, wherein the second vector arithmetic unit is a dedicated vector subtraction unit.

29. (Newly Added) The apparatus of claim 24, wherein a dynamically scalable vector conditional negate and add operation is performed within a single clock cycle by the first vector arithmetic unit.